

# Multi-Channel, Constant-Current Power Source for Aircraft Applications

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**Abstract:** To address the anticipated need of constant-current power sources in aerospace applications, we have developed a 3-kW, multi-channel source powered from a 3-phase, 400-Hz, 115-VAC supply. Special considerations impacting this design were minimizing volume, maintaining system power quality, and providing electrical fault protection. Performance results and a discussion of the design approach are presented.

**Keywords:** power-factor correction; constant-current source; 400-Hz power; aircraft power

## Introduction

We discuss the development of a 16-channel, 3-kW, constant-current power distribution unit (PDU) for aircraft applications. Electrical loads, such as lighting, de-icing heaters, and actuators may be operated from this compact power conversion unit. Because of the nature of aircraft systems, two of the most important design considerations are the maintenance of electrical power quality and minimization of weight. To this point, military and commercial standards for power quality are well established in MIL-STD-461F, MIL-STD-704F, Def-Stan 59-41, RTCA DO-160F, EUROCAE/ED-14D. At an operating power of 3 kW, an equipment designer must give special consideration to maintaining power quality according to the selected standard(s) and a power-factor correction (PFC) circuit will be needed to preserve the power quality of the AC source feeding the converter. To our dismay, the majority of PFC product development has been focused on 60-Hz systems as demonstrated by the lack of 400-Hz products. Astrodyne-TDI offers a single-phase, 375-W PFC [1] that operates over the input frequency range of 47 to 880 Hz. VICOR has a 1.4-kW, single-phase PFC [2] operating over the range of 47 to 440 Hz. However, this unit is not recommended for new designs and neither product was an optimal solution for the present application. Fortunately, SynQor produces a 1.5-kW, 3-phase, PFC operating over the range of 45 to 800 Hz [3] which became commercially available in July 2016.

## PDU Topology

The functional block diagram of the PDU is shown in Figure 1. Primary power is supplied by the platform's 3-phase, 115-VAC, 400-Hz bus while all other housekeeping power is derived from the 28-VDC bus. The primary power is conditioned by SynQor electro-magnetic interference filter (EMI) and PFC modules. Two EMI modules (MACF-115-

3PH-UNV-HT) and two PFC modules (MPFC-115-3PH-270-FP) are used in combination to produce a nominal 275-VDC source with power quality conforming to MIL-STD-704F and MIL-STD-461F specifications. The 275-VDC power is distributed among the 16 constant-current output converters. The outputs of the 2 pairs of filter-PFC modules are not directly interconnected, each PFC module powers 8 channels. Each output channel is comprised of a DC-DC buck controller (Microchip, HV9661), a DC ground-fault (GF) detector, an output voltage monitor, and an isolation relay. Presently, a maximum output current of 1 A may be supplied by each channel. The operation of the PDU is controlled by a 16-bit microcontroller (Microchip, PIC24F32KA304) and a variety of other circuits that support signal processing, platform-PDU communications, and built-in test (BIT) functions.

In one typical operating scenario, the BIT would be performed as part of the power-up sequence. This test verifies the operational status of the analog measurement circuits and other functional blocks. Upon successfully completing the BIT, the user would program operational parameters. As previously stated, the PDU channels are arranged as 2 groups of 8 channels where the output current level may be set on a per-group basis. Otherwise, each channel has independent enable/disable control, ground-fault detection, output voltage monitoring, and galvanic load isolation. Also, that in the case of catastrophic failure, the 275-V supply is fuse-protected at each channel. A few of the salient design features of the PDU are presented below.

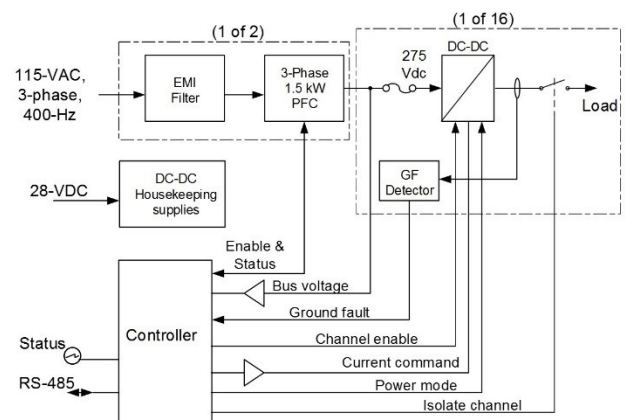
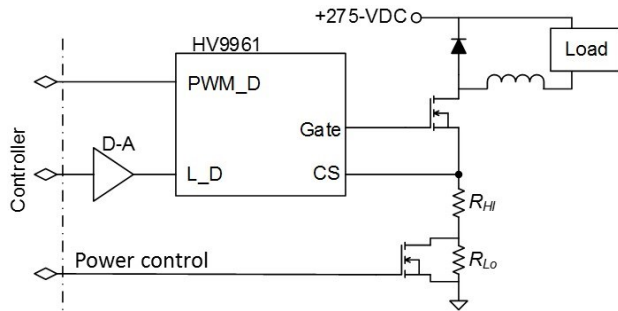


Figure 1. Power Distribution Unit simplified functional diagram.

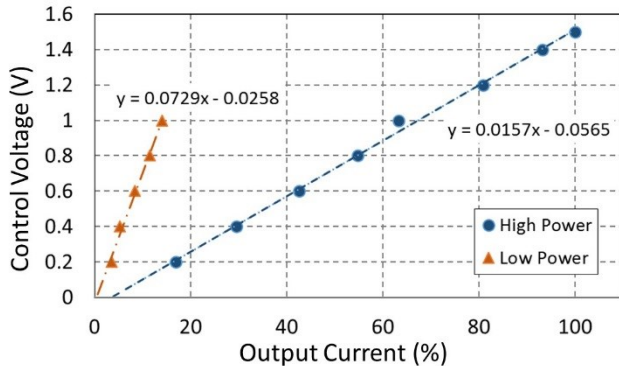
### Constant-current Converter

The HV9961 average-mode, buck controller is very attractive for this application because it supports high-frequency switching, includes both analog and digital adjustments of the output current, and output over-current protection. A simplified schematic of the buck converter used for each constant-current channel is shown in Figure 2. As documented in its data sheet [4], the current used to energize the buck inductor is monitored as a voltage at the Current Sense (CS) input through a current-sensing resistor and is the control feedback signal. The control scheme holds the Gate output off-time constant and the switching



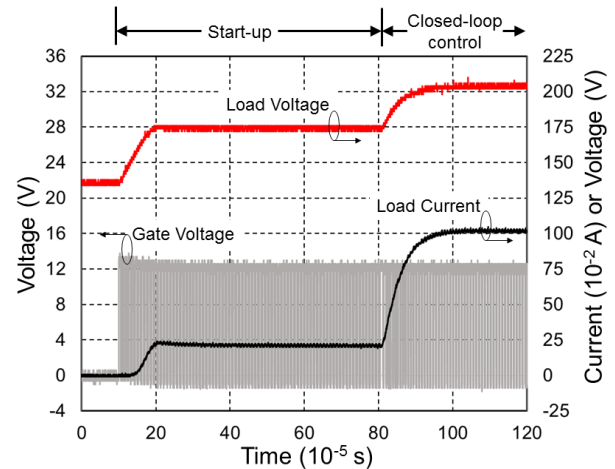
**Figure 2.** Simplified schematic of the HV9961 buck converter.

frequency is adjusted to regulate output current. The output current set-point may be adjusted by applying a voltage on the linear dimmer ( $L\_D$ ) input in the range of 0 to 1.5 V. A fixed off-time of 2  $\mu$ s was chosen for this design and this dictates a buck duty-factor range of 0.33 to 0.75 which translates to an output current range of 0.17 to 1.0 A. To extend the range to lower currents, the current sensing resistor was split into two components,  $R_{Hi}$  and  $R_{Lo}$ , and a shunt-transistor, under microprocessor control, modulates the resistance value. Lower currents may be obtained by turning off the shunt transistor. Figure 3 shows the ranges of output currents available in the two modes. In low-power mode,  $L\_D$  may be varied to give a range of currents from 39 mA (4%) to 140 mA (14%) and in high-power mode, 170 mA (17%) to 1 A (100%).



**Figure 3.** Output current as a function of the dimmer control voltage for the high- and low-power modes.

One control issue arises from the HV9961's over-current protection scheme. We found that high current set-points could only be achieved by modulating the logical dimming input ( $PWM\_D$ ) during the start-up period. By disabling the gate driver, via  $PWM\_D$ , the over-current detection circuit was effectively "reset" and the built-in over-current off-time of 400  $\mu$ s could be significantly reduced thereby allowing the DC output current in the buck inductor to increase. The start-up waveforms for maximum output current are shown in Figure 4. During the time between 10  $\mu$ s and 81  $\mu$ s,  $PWM\_D$  is switched by the microcontroller. Based on this signal, the HV9961 produces a gate drive pulse train at a frequency of 111 kHz and having a duty factor of 0.58. This waveform was empirically optimized for low-current start-up, but is used for all current levels in this prototype system. In Figure 4, the output current saturates at approximately 220 mA at 20  $\mu$ s. At this level, the converter could have been placed under closed-loop control without a current fault. In the present example, when open-loop control is relinquished at 81  $\mu$ s,  $PWM\_D$  is held active and the buck controller attains current regulation, at approximately 106  $\mu$ s, through closed-loop control without experiencing an over-current condition. At an output current of 1 A, the steady-state gate switching frequency is approximately 130 kHz. Note also in Figure 4 that the initial output voltage (when there is no switching) is approximately 137 V. This is due to the relatively high load resistance and leakage current flowing through the power transistor.

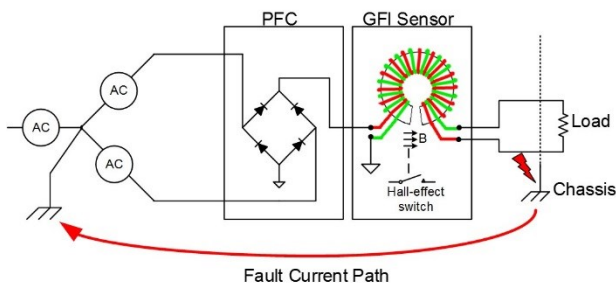


**Figure 4.** Load voltage and current waveforms during start-up of the HV9961 buck controller.

### Ground-fault Sensor

Because the PFC-rectifier module does not provide galvanic isolation, there exists a possibility that a ground-fault event could damage the PDU. Figure 5 shows a simplified schematic of a drive channel and potential fault scenario. In normal operation, the channel is isolated from the platform chassis and the load current passes to and from the PFC through a bifilar-wound, gapped toroid core (EPCOS, B64290L38X38). With equal (and opposite) winding currents, the instantaneous flux in the toroid core is zero.

However, if one of the load's terminals experiences a short-circuit to chassis, for example, or an arcing event occurs, the net current through the windings will not be zero and a flux will be generated. A Hall-effect switch (Allegro Microsystems, A1120), with an operating point of 3.5 mT, is inserted in the toroid gap and, in this design, will respond at a differential current of 200 mA. If any of the GF sensors reports a fault, logic within the control system will identify and isolate the appropriate channel(s) then notify the microcontroller through a hardware interrupt.



**Figure 5.** Simplified schematic of the ground-fault detection scheme.

#### *Mechanical Configuration*

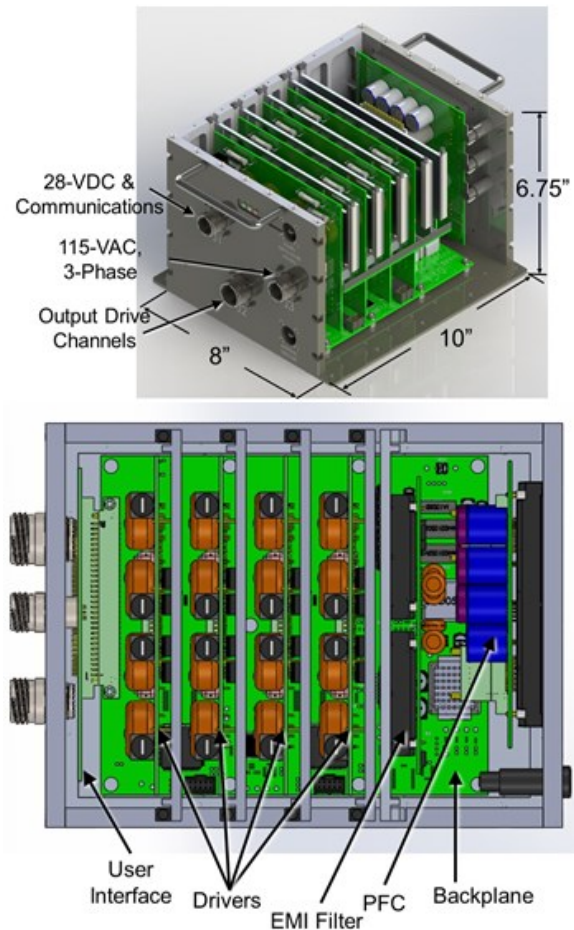
Figure 6 shows the solid model of the constant-current, PDU which has a volume of 540 in<sup>3</sup> and a weight of approximately 16 lbs. The PDU is constructed as a motherboard with function-specific daughter-cards. The control processor, complex programmable logic devices, analog interface circuits, and housekeeping power converters are located on the backplane circuit card (motherboard) which is positioned on the bottom of the chassis. Each of the 4 drive cards contains 4 constant-current output channels and has an aluminum plate that transfers waste heat to the chassis through wedge-lock card retainers. The user-interface card is also connected to the motherboard and contains the front-panel connectors, isolated RS-485 communications interface, and status indicators. The PFC is mounted to the chassis' back panel to enhance heat removal.

#### **Summary**

We have presented an overview of the design requirements and engineering approach taken to realize a 3-kW, constant-current source compatible with 115-VAC, 400-Hz input power systems. Special considerations addressed in this design are maintaining system power quality and providing electrical fault protection. By manipulating the control parameters of a buck-mode controller, we demonstrate constant-current operation at 1 A and 200 V per channel.

#### **Acknowledgement**

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**Figure 6.** Rendered solid model of the Power Distribution Unit and identification of major system components.

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